Microstrip and Grounded CPW Calibration Kit Comparison for On-Wafer Transistor Characterization from 220 GHz to 325 GHz

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***Abstract*—In this paper, we investigate the effect of two calibration errors, probe placement and capacitance per unit length, on transistor characterization, from 220 GHz to 325 GHz, on both a microstrip and an inverted coplanar waveguide with a via-stitched ground plane (CPW-G) calibration kit. We find that the calibration errors tend to be greater for the microstrip calibration than for the CPW-G calibration. These findings have critical ramifications for transistor characterization and modelling, and active circuit design.**

Keywords—calibration, on-wafer, uncertainty, microstrip, coplanar waveguide, HBT, common emitter, common base, WR 3.4

I. Introduction

With the increasing demand for communication devices operating in the sub-millimeter wave regime, companies have developed transistor technologies [1], [2] that operate at terahertz (THz) frequencies. First-pass design success at these frequencies requires accurate models of the transistors, requiring accurate measurements for model extraction and validation [3]. As seen in [4], the uncertainty in the transistor model has major impact on the power amplifier design and thus better characterization methods and transistor model extraction approaches are still needed at millimeter wave and terahertz frequencies. In multi-stage power amplifier design, deviations from the optimal impedance terminations can lead to decibels (dB) of difference in gain, loss in percentage points of power-added efficiency, and unstable designs.

Vector network analyzer (VNA) S-parameter measurements require correction via on-wafer calibrations to move the reference plane to the device-under-test on the wafer. The multi-line Thru-Reflect-Line algorithm (mTRL) [5] with impedance transformation to a 50 Ω system is a robust calibration method that has been successfully demonstrated for characterizing transistors up to 750 GHz [6] and is used as the calibration algorithm for this paper. Here, we investigate the effect of two uncertainty sources, probe placement error and capacitance per unit length variation, on transistor S-parameter measurements calibrated with two different mTRL calibration kits. We propagate these uncertainties onto common-emitter (CE) and common-base (CB) heterojunction-bipolar-transistor (HBT) measurements to show how the calibration kit selection affects the accuracy of the resulting S-parameter transistor measurements and characterization metrics such as K factor and maximum available gain (MAG).

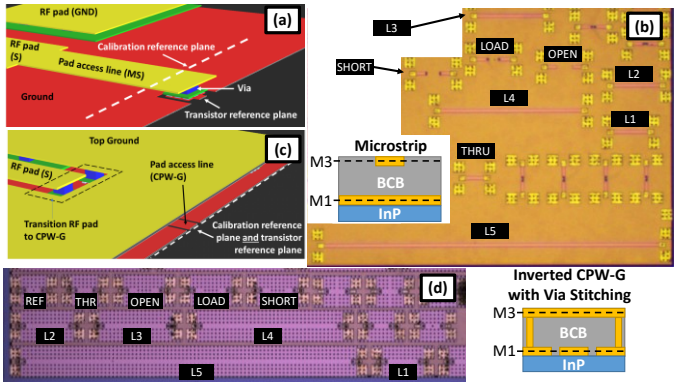

Fig. 1. On-wafer calibration kits for transistor characterization (a) 3D illustration of the microstrip access pad (b) Photograph of the microstrip calibration kit and its transmission line cross section (c) 3D illustration of the CPW-G access pad (d) Photograph of the CPW-G calibration kit and its transmission line cross section.

II. On-Wafer mTRL Calibrations

A. Microstrip and Inverted Grounded CPW Calibration Kits

We designed two different mTRL calibration kits to characterize on-wafer devices, including transistors. The first calibration kit, shown in Fig. 1 (a) and Fig. 1 (b), is a microstrip calibration kit that has the signal on the top plane metallization and the ground on the bottom plane metallization with a benzocyclobutene (BCB) layer separating the signal and ground. The access line from the ground-signal-ground (GSG) contact pads to the transistor reference plane is shown in Fig. 1 (a). Notably, the calibration reference plane and the transistor reference plane are separated by a via which will require additional measurements or an approximation of the structure in simulation to move the calibration reference plane to the transistor reference plane.

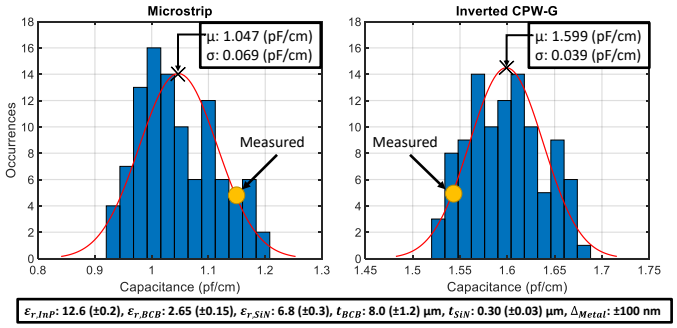

Fig. 2. Histograms of the capacitance per unit length from simulation with manufacturer's tolerance. Red solid lines are the Gaussian distribution fit to the histogram. Yellow dots indicate capacitance determined through measurement. Geometric and material tolerances used in simulation are shown at the bottom.

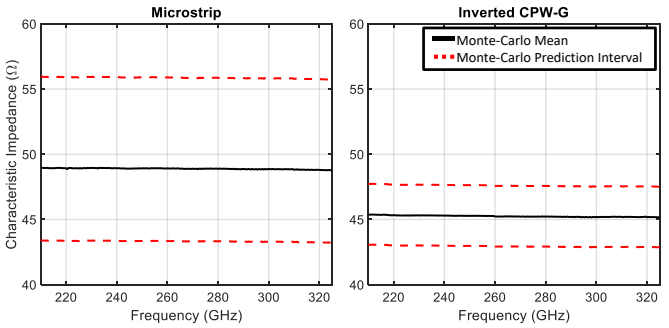

Fig. 3. Characteristic impedance of the transmission lines from the measured propagation constant with the simulated capacitance per unit length variation.

The second calibration kit, shown in Fig. 1 (c) and Fig. 1 (d), utilizes an inverted coplanar waveguide grounded (CPW-G) with via stitching from the top plane ground to the CPW ground on the bottom plane metallization. This type of CPW-G structure was originally used to reduce parasitic inductance in the ground connections of THz common-base amplifiers [9] and THz amplifiers that were characterized up to 550 GHz with this CPW-G calibration kit [7], [8]. The CPW-G structure suppresses resonances from neighboring lines that can be excited by surface wave propagation [10] and direct probe coupling [11]. The calibration standards can consequentially be safely placed in a compact area unlike the microstrip calibration kit which requires more space between the standards.

Unlike the microstrip calibration kit, the inverted CPW-G calibration kit is designed to directly characterize the transistor without the parasitic effect of the via as shown in Fig. 1 (c). Therefore, the calibration reference plane is directly set to the reference plane of the transistor. Each calibration kit contains five lines, a thru, and a short standard for the mTRL calibration, as well as open and loads for calibration verification.

B. Simulation of the Capacitance per Unit Length of the Line

The mTRL algorithm [5] requires an estimate for the capacitance per unit length of the transmission line in order to transform the reference impedance to 50 Ω [12]. This method is applicable assuming a substrate with negligible loss. We used a commercial EM simulator to estimate this capacitance value from a 2D cross section of the microstrip and inverted CPW-G transmission lines. We varied the effective permittivities and thicknesses of the BCB, InP, and SiN materials as well as the dimensions of the metal lines according to the tolerances described in [6] and included the values at the bottom of Fig. 2. Variations in material properties and geometry arise during the manufacturing process. These parameters were varied randomly, each with a uniform distribution, across 100 Monte Carlo simulations to obtain the histograms shown in Fig. 2. From this data we see that the sample standard deviation (σ) of the capacitance for the microstrip transmission line was 77% greater than the standard deviation of the inverted CPW-G capacitance, which will have significant ramifications for the measurement uncertainty. We also measured the capacitances per unit length of the transmission lines based on the measurement of a load [13]. The measured microstrip capacitance was 1.14 pF/cm and the CPW-G capacitance was 1.54 pF/cm and are displayed as yellow dots in Fig. 2. Note that these estimates may also vary across the wafer due to process variation and rely on an accurate measurement of the DC resistance of the load.

C. On-wafer Calibration and Verification

We used WR3.4 extender heads connected to a VNA and measured S-parameters from 210 GHz to 325 GHz with a 500 MHz frequency step. The probes were landed manually for all measurements with an approximate probe landing error of +/- 10 um. Each raw measurement was stored and corrected later in post-processing using the mTRL calibration algorithm in the Microwave Uncertainty Framework (MUF) [14].

We performed two 200 Monte Carlo iterations using the MUF, one that randomly varied only the capacitance per unit length value and one that randomly varied only the probe-tip placement distance, to propagate these variations as uncertainties to calibrated S-parameters. A Gaussian distribution was used for both error mechanisms. The probe placement error, which accounts approximately for the changing capacitance and inductance of the landing pads [14], was applied directly to the model in each of the standards defined in the MUF. We do not consider any other sources of uncertainty such as VNA drift or process variation in the calibration standards. In this paper, the probe placement error and capacitance errors are described as uncertainties but in practice, using a fixed value for the capacitance and the probe placement error will create an error in their measurements that will propagate into any extracted model. We report the Monte Carlo standard deviation multiplied by two (2σ), also called the prediction interval (PI), as the uncertainty.

The mTRL algorithm solves for the propagation constant during the calibration, which we then use to determine the characteristic impedance of the transmission line [12]. Figure 3 shows the characteristic impedance for both the microstrip and inverted CPW-G with uncertainties due only to variations in the capacitance per unit length. At 320 GHz, the microstrip has a characteristic impedance (Z_0) of 48.8+/- 6.3 Ω and the CPW-G has a Z_0 of 45.2+/-2.3 Ω. Clearly, the microstrip has greater uncertainty than the CPW-G since the BCB thickness variation directly affects the capacitance on the microstrip transmission line. At this point we already see the resilience of the CPW-G

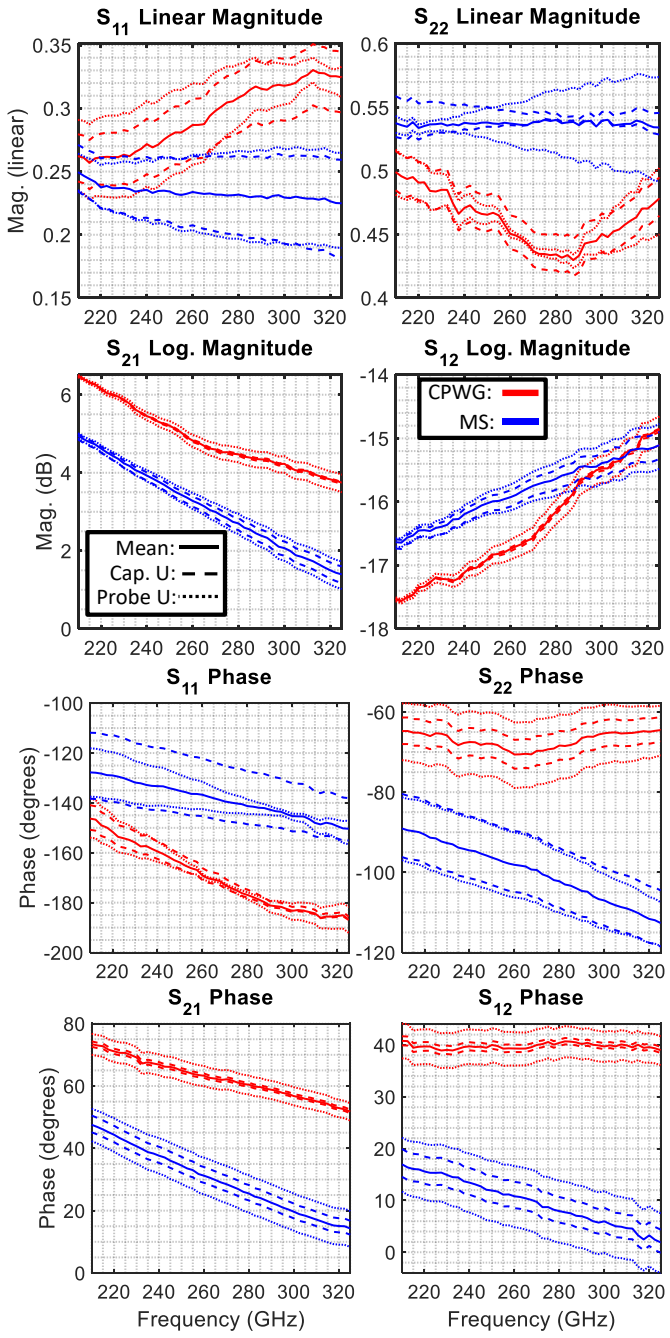

Fig. 4. Measured scattering parameters of a 4 µm Common Emitter HBT with a microstrip (blue cruves) and a CPW-G (red curves) calibation kits. The solid line corresponds to the Monte Carlo mean value. The dashed line corresponds to the uncertainty on the value from the capacitance error. The dotted line corresponds to the uncertainty from the probe placement error. Microstrip HBT bias point: V_{ce} = 1.8 V, J_e = 19.2 mA/µm^2. CPW-G HBT bias point: V_{ce} = 1.8 V, J_e = 19.2 mA/µm^2.

calibration kit to process variation but we will now demonstrate how this uncertainty impacts transistor measurements.

III. Characterization of Common-Emitter Transistors

We applied the mTRL calibrations to on-wafer measurements of a single-side collector (SSC) 4 µm Common-Emitter (CE) HBT with the microstrip access line and one with the CPW-G access lines, both with approximately the same bias point of V_{ce}: 1.8 V, J_e: 19.2 mA/µm^2. The corrected S-parameters of the transistors are shown in Fig. 4, where the microstrip calibration is shown in blue while the inverted CPW-G calibration is shown in red. The solid line shows the mean of Monte Carlo result. The dashed line indicates the uncertainty resulting from the capacitance variation and the dotted line indicates the uncertainty resulting from probe placement error. The S-parameters of the HBT are different for the microstrip and CPW-G calibrations since the microstrip calibration kit does not de-embed the via that connects the signal to the transistor. Also, the transistors in the microstrip and CPW-G have different electromagnetic environments. Table I explicitly lists the differences between the upper and lower PI at 220 GHz and 320 GHz. We highlighted the largest differences, with red font in the linear magnitude and every phase value above 10 degrees.

The uncertainty in the linear magnitude of S_{11} and S_{22} is similar for both calibration kits, however, there is significant difference in the phase across all S-parameters. For both reflection coefficients, the microstrip line has capacitance uncertainty that is similar to or much greater than the probe uncertainty. At 220 GHz, we observe that the difference in the upper and lower PI of S_{11} phase, due only to capacitance variation, for the microstrip case has over a 26.8° difference while the CPW-G calibration has an 8.9° difference. The CPW-G calibration exhibits a much lower phase variation due to the capacitance uncertainty than the microstrip across all frequencies. The phase of the S_{22} plot shows the probe uncertainty as significantly greater than the capacitance uncertainty. In the S_{21} and S_{12} phase plots, the phase uncertainty due to the capacitance is lower for the CPW-G than the microstrip. The impact of probe placement uncertainty is greater than the capacitance uncertainty for both cases across all frequencies.

IV. On-Wafer Characterization of Common-Base Transistors with Ground Inductance Variations

The previous section demonstrated the lower uncertainty for the CPW-G structure, which we now use in this section to accurately characterize important figures of merit of CB HBTs. The CB transistor is often preferred over the CE topology due to its higher MAG in the THz frequency bands, although the linear stability characteristics of the CB topology may be highly disrupted with small variation in the base feed inductance and the emitter overlap capacitance [15]. We measured three 3 um emitter-length CB HBTs with different ground connections using the CPW-G calibration kit with a bias point of V_{cb} = 1.0 V, J_e = 20 mA/µm^2. To reduce the base inductance, the first device uses a double base post connection (L_B/2) while the second uses a single base post connection (L_B). A 5.5 um line length is inserted on the ground connection to intentionally add a 1.9 pH parasitic inductance, resulting in a total base inductance of L_B + 1.9 pH. The measured K factor and MAG of these transistors are shown in Fig. 5, which shows only the probe positioning in the shaded region as both metrics are immune to capacitance variation uncertainty. The probe positioning uncertainty was negligible for the MAG metric. We were successfully able to observe the K stability factor and the MAG decreasing with increasing base inductance.

TABLE I.

DIFFERENCE IN THE UPPER AND LOWER PREDICTION INTERVALS

Uncertainty of S-parameters at 220 GHz & 320 GHz	Microstrip		Inverted CPW-G	
	Cap M.C P.I. Δ	*Probe M.C P.I. Δ*	*Cap. M.C P.I. Δ*	*Probe M.C P.I. Δ*
220 GHz				
S_{11} Linear Mag.	0.03	0.05	0.04	0.06
S_{22} Linear Mag.	0.04	0.02	0.03	0.03
S_{21} & S_{12} Mag. (dB)	0.08	0.33	0.13	0.11
S_{11} Phase (deg.)	27.91	10.74	8.90	13.39
S_{22} Phase (deg.)	14.74	14.03	6.66	14.71
S_{21} & S_{12} Phase (deg.)	5.74	10.38	1.68	6.72
320 GHz				
S_{11} Linear Mag.	0.07	0.05	0.05	0.02
S_{22} Linear Mag.	0.01	0.08	0.03	0.05
S_{21} & S_{12} Mag. (dB)	0.38	0.64	0.05	0.44
S_{11} Phase (deg.)	18.87	18.07	1.64	9.67
S_{22} Phase (deg.)	13.72	5.23	6.24	13.00
S_{21} & S_{12} Phase (deg.)	5.18	8.94	1.17	5.67

V. DISCUSSION & CONCLUSION

The microstrip and inverted CPW-G calibration kits are both affected by the same manufacturing tolerances and process variations but the microstrip calibration kit results in greater capacitance variation than the CPW-G kit. The probe placement variation also contributes significant uncertainty to both the microstrip and CPW-G calibrations and must be mitigated through precise probe positioning. In compact transistor modeling, the modeler fits the intrinsic and extrinsic characteristics to the measured S-parameters of the transistor in various bias configurations. Thus, the uncertainty in the magnitude and phase of the S-parameters directly affects the precision of an extracted model. The measured results of the CB HBTs also show that we can accurately detect small differences in the transistor ground connections and show how these differences affect their figures of merit.

By choosing the inverted CPW-G, transistor measurements have greater resilience to fabrication errors, a calibration reference plane nearer to the transistor terminals, and less measurement uncertainty. The CPW-G also leads to more precise load pull characterization of transistors as these measurements require accurate magnitude and phase. This makes the inverted CPW-G a better choice for accurate transistor characterization and transistor model verification. The next step is to see if these measurements are accurate enough to detect process variation between transistors and to extract transistor models at these frequencies.

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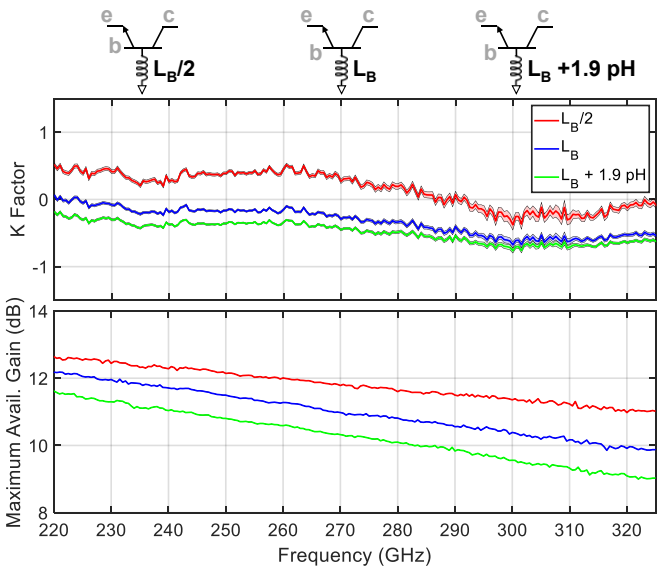

Fig. 5. Measured stability factor and maximum available gain of a 3 µm Common Base HBT with three different base inductances resulting from the ground connections. Shaded area around curve denotes the uncertainty. For all cases, the bias point: V_{cb} = 1.0 V, J_e = 20 mA/µm^2

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